A 900 MHZ IMAGE-REJECT TRANSCEIVER SI BIPOLAR IC

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ABSTRACT

An ISM-band transceiver chip includes an LNA, image-reject up- and down-converters, a VCO, a /64,/65 dual-modulus prescaler, an IF Limiting amplifier/ RSSI strip, and a voltage regulator. The IC operates from a single-supply down to 3.0 V and is optimized for a 10.7 MHz IF frequency to allow use of very low-cost ceramic filters. The 6.8 mm^2 chip is fabricated using a 24 GHz f_T Si bipolar process and mounted in a 28 pin SSOP package.

INTRODUCTION

In the last few years, there has been fast-paced development of wireless digital communication systems to take advantage of changes in FCC rules [1] for non-licensed radio equipment. These rules allow substantial rf power (up to 1 W) and signal bandwidth to be transmitted in specified (ISM) frequency bands, provided appropriate spread-spectrum modulation techniques are used. They also relax spurious emission requirements with respect to those for narrow-band systems, thereby allowing greater flexibility in the choice of spread-spectrum radio architecture to reduce its cost.

In high-volume applications such as residential cordless telephones, radio implementation is driven by key requirements of minimizing cost, maximizing range, talk, and standby times while maintaining good voice quality, link security, high immunity to interference. Compared to currently prevalent analog phones, the high-power digital spread-spectrum systems are intrinsically well-suited for the longer-range, interference robustness and security requirements. However, their higher complexity make them particularly challenging to implement at low-cost, and the higher transmit power can lead to very large receiver input signal-range requirements due to near-far interactions in environments with multiple handsets or base stations.

The rf transceiver chip presented here was designed specifically to provide a compact, low-cost, high-dynamic range radio implementation for the 902-928 MHz unlicensed band, with no need for any "trims" [2]. It was optimized for a frequency-hopping digital cordless telephone application, to be used in conjunction with a CMOS baseband processor/controller IC which includes a digital 10.7 MHz, 93 kbps FSK modulator and demodulator [3].

SYSTEM ARCHITECTURE

Figure 1 shows a functional block diagram of the transceiver. One of its key feature is the single-conversion architecture which eliminates the need for the additional synthesizer, VCO and filters required in dual-conversion radios, and enables the use of very low-cost ceramic filters widely available at the 10.7 MHz IF frequency. With this low IF, the image frequency falls within the allocated rf band and cannot be rejected by fixed center-frequency filters. Thus, image-rejection mixers with fully integrated quadrature phase-shift networks are used for both the receive down-conversion and transmit up-conversion.

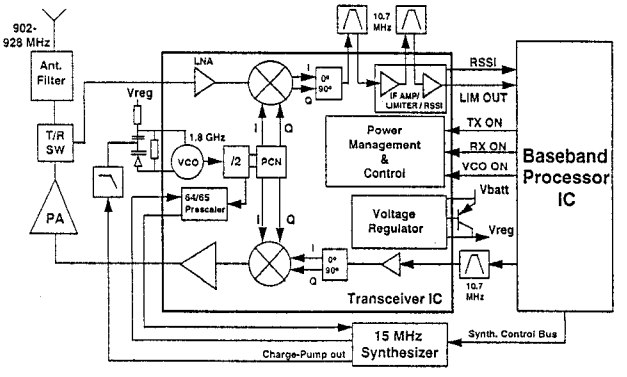

Figure 1: Block diagram of the low-IF ISM-band radio

The transceiver IC features an LNA, image-reject up- and down-converters, a VCO, a /64,/65 dual-modulus prescaler, an IF Limiting amplifier/RSSI strip, and a voltage reg-

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ulator. All these functions were designed into a 28 pin package to minimize assembly and test costs. The prescaler is used to drive a low-cost CMOS synthesizer chip to phase-lock the VCO to a crystal reference. An external PA boosts the transmit power to the desired output level, and a low-cost T/R switch enables time-division duplexing.

CIRCUIT DESIGN

The down-converter design was driven by the requirements for low noise figure, good image rejection, peak input signal levels in excess of +15 dBm, low second-order distortion (to minimize LO$\pm$1/2 IF responses) and high LO-RF isolation. Figure 2 shows a simplified schematic of the receive LNA-I/Q mixer. The LNA is realized using the Q1,Q2 cascode amplifier to provide high gain and LO isolation. It is followed by an on-chip planar transformer balun which drives a pair of doubly-balanced mixer cores (Q4-Q7, Q8-11). This topology provides larger output voltage-swing headroom compared to regular Gilbert-cell designs. Transistor Q1 at the LNA input acts as a shunt switch which is turned-on in transmit mode to prevent PA output rf leakage through the T/R switch from biasing-up the LNA or generating non-linearities which would pull the VCO. Image rejection is obtained through balanced IF quadrature phase combiners for the mixer I/Q outputs. These are implemented using a 2-section RC polyphase network [4,5].

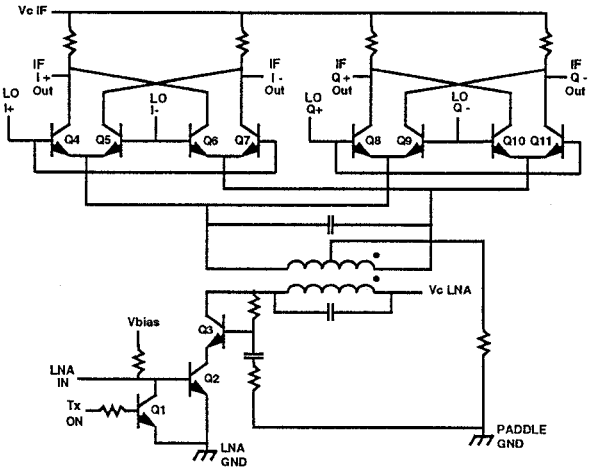

Figure 2: Simplified Schematic of the LNA-I/Q mixer

The transmit up-converter IF quadrature phase splitter was realized using a 3-section polyphase network. Heavy degeneration was used in both the IF amplifiers and the modified Gilbert-cell up-converter mixers to keep IF harmonic distortion low-enough to comply with FCC spurious emission limitations at 960 MHz and above. Simple external matching circuits at the LNA input, down-converter output, and transmit up-converter output provide $\leq$-10 dB return loss at all ports.

The balanced VCO circuit is similar in design to that described in [6]. It operates at twice the required LO frequency to minimizes pulling effects and allow generation of "coarse quadrature" signals at the LO frequency using a pair of latches clocked in anti-phase. The quadrature accuracy of this approach is typically limited by the second-harmonic content of the VCO signal, due in this case to the finite balance achievable with an external tank circuit (used to minimize phase noise). We improved this quadrature accuracy by using an RC phase-correction network (PCN in Figure 1) after the /2 circuit. To obtain high linearity while minimizing power consumption, separate up- and down-conversion mixer LO buffer circuits are enabled to deliver about 700 mVp-p differential LO swing to the mixer cores. A low-dropout voltage regulator circuit for the VCO was included on-chip, using an external pass-transistor, to minimize pushing effects from power-supply noise and transients. Its nominal output voltage of 2.75 V was chosen to allow the chip to operate from a single-supply voltage down to 3.0 V.

The /64,/65 dual-modulus prescaler operates at the LO frequency. It uses a /2,/3 high-speed synchronous input counter followed by a 5-bit ripple-counter extender with associated control logic. The counters are based on 3-level CML D-type flip-flops similar in design to those described in [7].

The 100 dB gain IF limiting amplifier strip is split into two sections, which allows an external filter to be inserted between them to limit noise bandwidth and enhance radio selectivity. Nominal 330 ohm IF filter terminations are integrated on-chip. On-chip ac inter-stage coupling eliminates the need for DC offset feedback loop and with its associated (typically large) decoupling capacitors. The logarithmic RSSI circuit uses an eight-stage successive detection architecture to provide a filtered signal strength indication voltage output with high log-linearity accuracy over a wide dynamic range. All except the first two detectors are linked to the amplifier stages in the second IF section so as to limit false readings from strong out-of band signals which are rejected by the interstage filter.

The supply and grounding scheme as well as pinout configuration (Figure 3) are critical to preventing undesirable interaction between the various circuits, particularly with the limited number of pins available and a desired receiver input sensitivity level around -105 dBm. Separate ground pins are used for the LNA input and PA output driver stages. The input differential pairs for both IF amplifier sections share a common ac ground reference pin.

This prevents instability due to common ground inductance/resistance and minimizes spurious noise pickup. The ground nodes for other circuit blocks are down-bonded to the die-attach paddle, which is grounded via three pins.

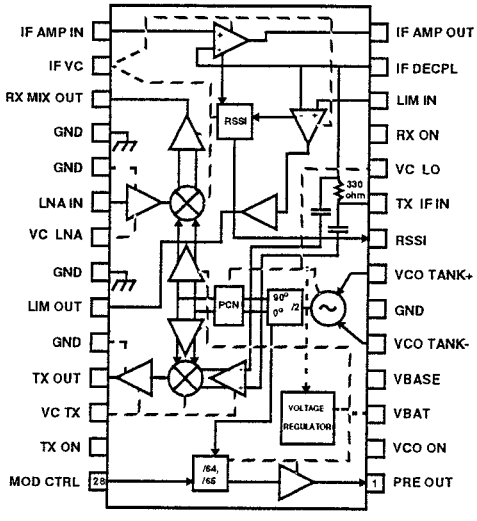

Figure 3: IC Pin configuration

Figure 4 shows a picture of the 103 x 103 mil^2 IC, which is fabricated using a 24 GHz f_T silicon bipolar process.

MEASURED PERFORMANCE

Figure 5 shows the RSSI output voltage vs. LNA input signal level, with external 10.7 MHz IF filters. Log-linearity is better than ± 3 dB over an 80 dB input power range. RSSI droop at higher input power levels is due to VCO pulling (VCO is free-running in this measurement, but in a radio with a suitable preamble period, the PLL re-centers the VCO frequency prior to active part of the data burst). A sensitivity of -105 dBm for 10^{-4} bit-error rate has been achieved for a radio prototype [1] in conjunction with the baseband processor IC described in [3]. Figure 6 shows the spectrum of the transmit upconverter output driver. Note the LO-3IF spur level is -58 dBc. This spur gets upconverted to an LO+5IF frequency through the limiting action of an external PA. However, with the selectivity available from a low-cost ceramic antenna filter (Figure 1), this level is adequate to meet FCC requirements with a PA output carrier power level of at least 25 dBm. Table 1 summarizes other key measured performance parameters of the transceiver chip over the ISM band, with a 10.7 MHz IF. The average receive image-rejection is 33 dB, with a standard deviation of 1.7 dB. Average transmit lower-sideband rejection is 48 dB with a standard deviation of 4 dB. These results are obtained from measurements on hundreds of chips over several

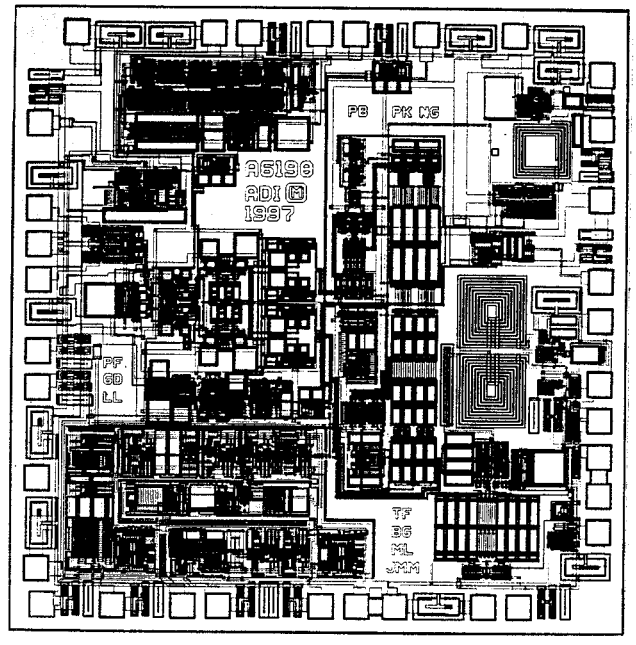

Figure 4: Die Photograph of the transceiver IC.

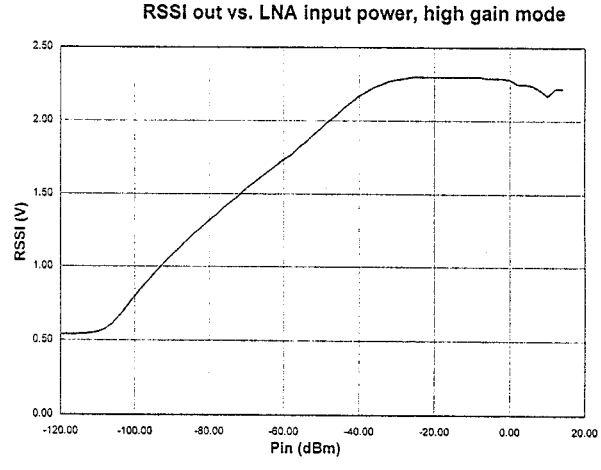

Figure 5: RSSI output voltage vs. LNA input power

fabrication lots, with no trimming either on- or off-chip.

CONCLUSION

An IC which integrates much of the RF and IF circuitry needed for an image-rejection 900 MHz transceiver has been implemented in a low-cost dual in line package. Excellent image-rejection performance was obtained without the need for any trimming. This IC provides a basis for realizing low-cost, high-performance ISM-band digital radios for applications such as cordless telephones.

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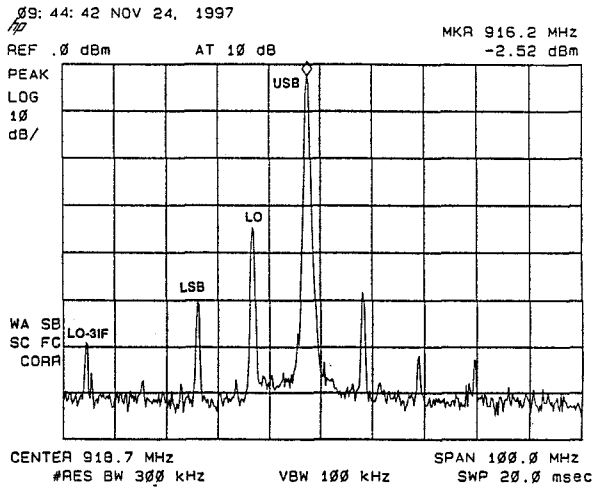

Figure 6: Typical up-converter output spectrum

Table 1: Typical IC Performance @ 25 °C

Parameter	Measured
LNA/Mixer:	
Conversion Gain:	24 dB
Lower-Image Rejection:	33 dB
Noise Figure:	4.2 dB
Input IP_3:	-17 dBm
Input IP_2 ($F_{RF} = F_{LO} + (F_{IF})/2$):	+16 dBm
LO feedthrough at RF port:	<-70 dBm
Transmit Upconverter:	
-1 dB Gain Compression o/p power:	+4.5 dBm
Power Gain:	18.5 dB
Lower-Sideband Rejection:	48 dB
LO feedthrough:	-33 dBm
Total Supply Current (Vc = 3.3 V):	
Receive Mode:	58 mA
Transmit Mode:	92 mA
VCO Mode (LO circuits, regulator, prescaler):	26 mA

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